STP tbd LF / ROD3827T2 @ 10.0MHz 5V

GPS Disciplined OCXO - PPS stand-alone oscillator module

1.0 Description

The ROD3827T2 is a High End OCXO made of embedded module synchronized and disciplined on 1PPS signal provided by the customer's GPS equipment.
It delivers an ultra-stable 10MHz sinewave frequency as well as 1PPS HCMOS output signal. Time and synchronization data are available through I^2C bus.

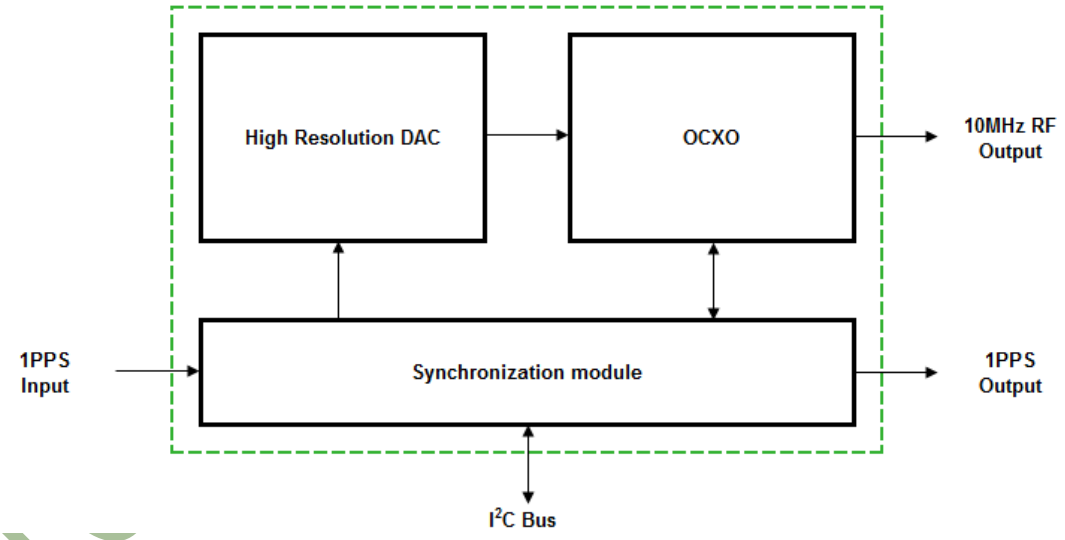
2.0 Application

- Grandmaster Clock
- Instrumentation

3.0 Main Features

- Holdover performance ≤ 1.5µs for 24h with external temperature variation ± 5°C
- Stability < 0.04ppb per 10°C variation over operating temperature range from -40°C to +85°C
- Package: 38 x 27 x 12 mm max
- 5V Single Power Supply
- 10 MHz sinewave output (possible HCMOS option)
- Internal locking function based on 1PPS from customer's GPS engine
- Cleaned 1PPS Output (on locked mode & 24 hours holdover mode)
- I^2C bus data communication

Block Diagram



4.0 Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Storage temperature	-45	95	°C
Supply voltage (Vcc)	-0.3	6	V
Voltage at any Digital Interface Pin with Respect to GND	-0.3	Vcc +0.3	V
Voltage on PPS Input	-0.3	Vcc +0.3	V
PPS Output current		5	mA
Load for sinewave RF output	45	55	Ω
Continuous output current for HCMOS optional RF output		± 50	mA

5.0 Power Supply

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Supply voltage (Vcc)	4.75	5.0	5.25	V	
Current consumption (at warm-up)			1000	mA	
Current consumption (in steady state)		400		mA	still air at 25°C
Power-on Recall Voltage	2.2			V	Minimum Vcc at which memory recall occurs
Vcc Ramp Rate	0.2			V/ms	

6.0 RF Output / Sinewave RF Output

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Waveform		Sinewave			
Load	45	50	55	Ω	
Output Power	5	7	9	dBm	
Harmonics			-30	dBc	
Spurious			-80	dBc	
Start-up time			1	Sec	

HCMOS RF Output Option

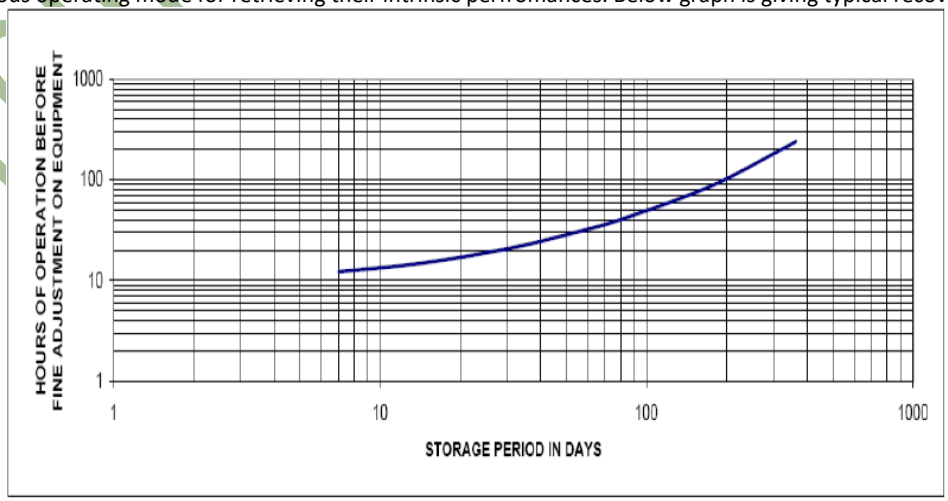
Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Waveform		HCMOS			
Low level output voltage (V_{OL})			0.4	V	
High level output voltage (V_{OH})	2.4			V	
Rise and fall times			5	ns	from 10% to 90% output levels, 15pF load
Duty cycle	45		55	%	At 50% level
Load		15	45	pF	

7.0 Temperature Range

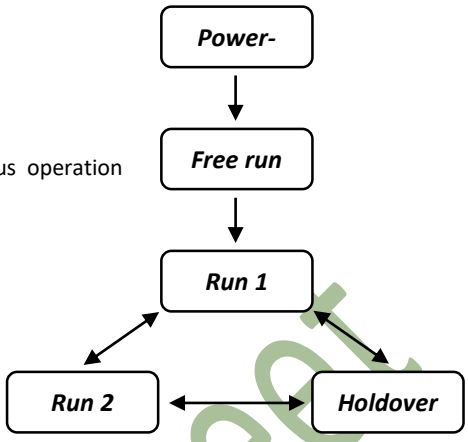
Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Operating temperature range	-40		+85	°C	Airflow speed between 1m/s and 3 m/s
Operable temperature range	-45		+90	°C	output signal available but not necessarily within the specified tolerances of frequency

8.0 Frequency Recovery

Frequency stability items of the device are measured before shipment. Then parts are shipped and could remain powered-off for an uncontrolled time, then assembled and tested over integration process. Parts could again remain powered-off until final installation in the application when the will operate in a continuous mode. Every time the parts are powered-off, everytime they will require continuous operating mode for retrieving their intrinsic perfromances. Below graph is giving typical recovery time:



9.0 Workflow Diagram



Power on

Free run **:** Featured stand-alone OCXO performances

Run 1 **:** Restricted mode, 30 minutes acquisition, frequency accuracy guaranteed

Run 2 **:** Full performance mode, phase accuracy is guaranteed after 4 hours of continuous operation

Holdover **:** 1PPS Input Signal turned off after suitable disciplining sequence (3 days min.), TIE is guaranteed

- *Warm-Up:*

That stage is corresponding to the initial operating mode of the device; it could occur after long powered-off time (storage, Integration & installation processes, etc.).
Due to frequency recovery phenomenon (see graph § 23.0), the device must be re-stabilized over continuous time of operation before reaching its overall intrinsic performances *(up to 10 days maximum after 1 year of storage – see § 23.0)*.

Stabilization steps & order of magnitude:
Start-up time within 1 second after powering-on the device; frequency signal output is delivered, within ppm of final frequency.
Power consumption will stabilize after a couple of minutes after powering-on at +25°C; that stabilization is dependent on ambient temperature at start (up to 5 minutes maximum at -40°C).

Temperature of the oven of the OCXO will be stabilized within less than 10 minutes at -40°C; but : no PPS output available at that stage.
Ageing slope will reach its final performance after recover time (see § 23.0).

- *Free run* :

Featured stand-alone OCXO delivering its intrinsic performances, except ageing slope (as it depends on the recovery phenomenon).
System stabilization process for preparing the data acquisition stage. No 1pps output.

- *Acquiring (Run-1)*

1pps input must be available for starting the process; it is lasting 30 minutes max. at -40°C after reset.
1pps signal input must be present over :

- the first 40 seconds and,
- 70% minimum of the remaining time, at any time;

if those conditions are not met, then back to free-run mode.
1pps output is acting after 50s after the 1pps input is available.

Short time loop. Able to handle system stabilisation. Start computing data for the locked mode.
On Hot system (after warm-up time), phase & frequency are tuned within a few minutes while Cold start require more time for the system to be stable enough (up to 30 minutes at -40°C).
When acquisition process is successful (30min. total time minimum):

- frequency accuracy is guaranteed within less than 1ppb;
- phase is aligned to the 1pps input signal.

- *Locked (Run-2)*

1pps input & 1pps output signals are available.
Optimized time loop. Get the best of the GNSS stability and the performances of the OCXO.
Acquiring ageing information.
Phase is locked, frequency is locked & guaranteed.
After 8 hours of continuous operation, phase accuracy is less than 100ns.

- *Holdover*:

after suitable disciplining sequence, TIE is guaranteed : 1pps input signal is not available; 1pps output signal is available.

Frequency stability over operating temperature is guaranteed.

After initial warm-up, system requires 3 days of continuous operation for meeting specified holdover stability.
The Holdover Time is guaranteed within half of the cumulated locked time, with a limit of 24 hours after 48 hours of locked mode minimum.

10.0 Different Running Modes

Parameter	Free Run	Run 1	Run 2	Holdover
Frequency calibration	Table 1	NA	NA	NA
10 years stability (over all)	Table 1	NA	NA	NA
Aging	Table 1	NA	NA	NA
Frequency stability over operating temperature range	Table 1	NA	NA	Table 4
Supply voltage stability	Table 1	NA	NA	Table 4
Load sensitivity	Table 1	NA	NA	Table 4
Acceleration sensitivity	Table 1	NA	NA	Table 4
Warm-up Time	Table 1	NA	NA	NA
Retrace	Table 1	NA	NA	NA
Phase Noise	Table 1	NA	Table 3	Table 4
Short Term Stability	Table 1	NA	Table 3	Table 4
1PPS Input	NA	Table 2	Table 3	NA
1PPS Output (see I²C recommendation § 150)	NA	Table 2	Table 3	Table 4
TIE	NA	NA	NA	Table 4

11.0 Free Run Mode – Table 1

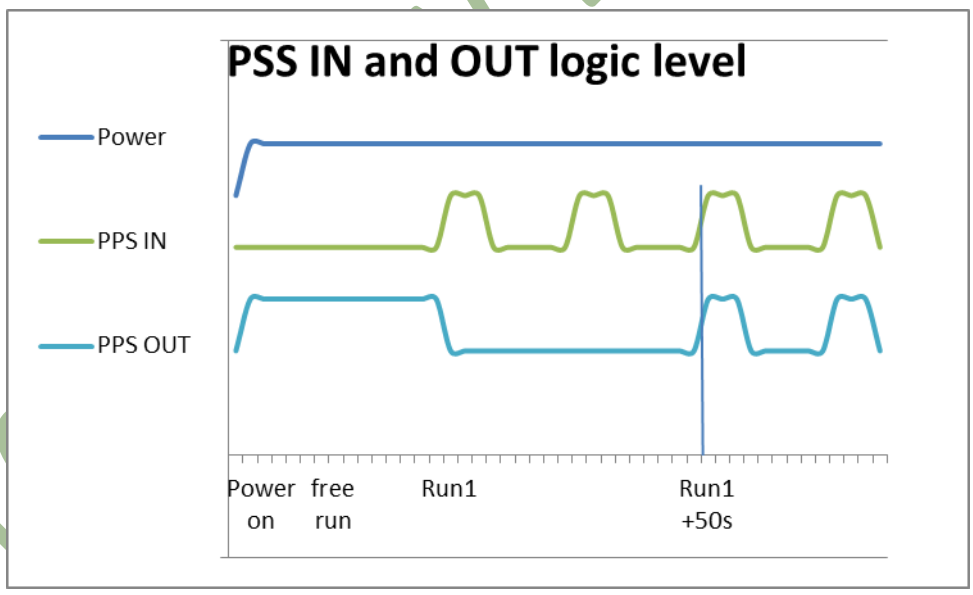
Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		10.0		MHz	
Frequency calibration (at +25°C ± 2°C)	-50		+50	ppb	at time of shipment, with reference to nominal frequency [1]
10 years stability (overall after recovery)			±350	ppb	Typical : 14 days of continuous operation
Aging (at shipment / after recovery time)					See § 23.0
per day			±0.2	ppb	Measured before shipment
per year			±50	ppb	Cumulated (extrapolation)
for 10 years			±300	ppb	Cumulated (extrapolation)
Frequency stability over operating temperature range			0.5	ppb	Reference to (Fmax - Fmin)
Frequency stability per 10°C variation			0.04	ppb	Over operating temperature range
Supply voltage stability	-0.25		+0.25	ppb	Nominal VCC ± 5% variation
Load sensitivity	-0.1		+0.1	ppb	50 Ω ± 10% variation
Acceleration sensitivity	-3		+3	ppb/g	Vs static orientation
Warm-up time to within ± 10ppb @ +25°C @ -40°C			3 5	minute minute	with reference to final frequency after 1h of continuous operation
Retrace Vs operating temperature range		±1	±5	ppb	24h on, 24h off, 1h on
SSB Phase Noise					Static conditions
1Hz		-100	-90	dBc/Hz	
10Hz		-130	-120	dBc/Hz	
100Hz		-145	-140	dBc/Hz	
1kHz		-150	-145	dBc/Hz	
≥ 10kHz		-155	-150	dBc/Hz	
Short Term Stability (ADEV)					Static conditions
1s to 100s		3	5	ppt	
1,000s		3	7	ppt	
10,000s		10	20	ppt	

[1] The characteristics of the OCXO may be temporarily affected by the processes of assembly and soldering. The frequency specifications apply 48 hours after assembly. Nominal conditions apply unless otherwise stated

12.0 Run 1 Mode – Table 2

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		10.000		MHz	
1PPS Input					
Waveform compatibility		HCMOS			
Low level input voltage (VIL)	0		1.2	V	
High level input voltage (VIH)	2.8		4	V	
Pulse width	10			µs	
Time deviation (TDEV)					
Tau = 1s		0.5	2	ns	
Tau = 10s		3	10	ns	
Tau = 100s		20	90	ns	
Tau = 1000s		20	90	ns	
Tau = 10000s		20	90	ns	
1PPS Output (see I²C recommendation § 15.0)					Available 30s max. after locking on 1PPS Input and over 24h in holdover mode
Waveform		HCMOS			
Low level output voltage (VOL)			0.4	V	Load 15pF // 10kΩ min
High level output voltage (VOH)	2.8		4	V	Load 15pF // 10kΩ min
Pulse Width		25		ms	
Rise and fall time			5	ns	10% to 90% level, 15pF load

- The phase alignment is done on the positive edge of both pps in and out signals .



13.0 Run 2 Mode – Table 3

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		10.0		MHz	
SSB Phase Noise					Static conditions
1Hz		-100	-90	dBc/Hz	
10Hz		-130	-120	dBc/Hz	
100Hz		-145	-140	dBc/Hz	
1kHz		-150	-145	dBc/Hz	
≥ 10kHz		-155	-150	dBc/Hz	
Short Term Stability (ADEV)					Static conditions
Tau = 1s to 100s		3	5	ppt	
Tau = 1000s		6	10	ppt	
Tau = 10000s		4	7	ppt	
1PPS Input					
Waveform compatibility		HCMOS			
Low level input voltage (VIL)	0		1.2	V	
High level input voltage (VIH)	2.8		4	V	
Pulse width	10			µs	
Time deviation (TDEV)					
Tau = 1s		0.5	2	ns	
Tau = 10s		3	10	ns	
Tau = 100s to 10,000s		20	90	ns	
1PPS Output					See I²C recommendation § 15.0
Waveform		HCMOS			
Low level output voltage (VOL)			0.4	V	Load 15pF // 10kΩ min
High level output voltage (VOH)	2.8		4	V	Load 15pF // 10kΩ min
Pulse Width		25		ms	
Rise and fall time			5	ns	10% to 90% level, 15pF load
PLL accuracy	-50		50	ns	After 4 hours disciplining

- The phase alignment is done on the positive edge of both pps in and out signals .

14.0 Holdover Mode – Table 4

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		10.000		MHz	
Frequency stability over operating temperature range			0.5	ppb	Reference to (Fmax - Fmin)
Frequency stability per 10°C variation			0.04	ppb	Over operating temperature range
Supply voltage stability	-0.25		+0.25	ppb	Nominal VCC ± 5% variation
Load sensitivity	-0.1		+0.1	ppb	50 Ω ± 10% variation
Acceleration sensitivity	-5		+5	ppb/g	Vs static orientation
SSB Phase Noise					Static conditions
1Hz		-100	-90	dBc/Hz	
10Hz		-130	-120	dBc/Hz	
100Hz		-145	-140	dBc/Hz	
1kHz		-150	-145	dBc/Hz	
≥ 10kHz		-155	-150	dBc/Hz	
Short Term Stability (ADEV)					Static conditions
Tau = 1s		3	5	ppt	
Tau = 10s		3	5	ppt	
Tau = 100s		3	5	ppt	
Tau = 1000s		3	5	ppt	
Tau = 10000s		6	10	ppt	
1PPS Output (see I²C recommendation § 15.0)					Available over 24 hours max. from holdover mode start
Waveform		HCMOS			
Low level output voltage (V_{OL})			0.4	V	Load 15pF // 10kΩ min
High level output voltage (V_{OH})	2.8		4	V	Load 15pF // 10kΩ min
Pulse Width		25		ms	
Rise and fall time			5	ns	10% to 90% level, 15pF load

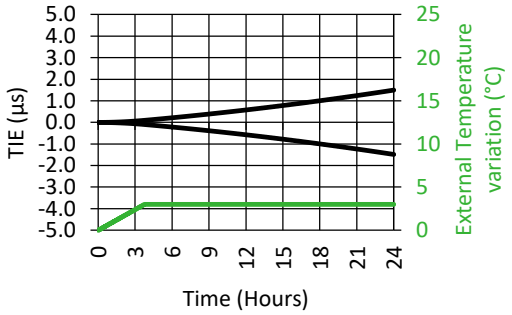
15.0 Holdover Mode Continued

TIE (Time Interval Error) :

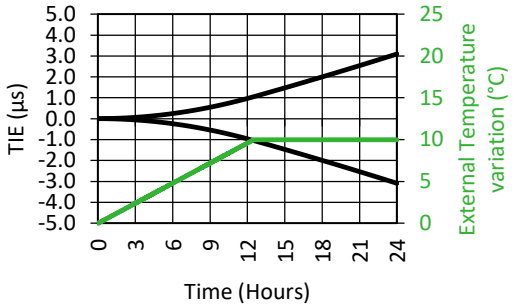
Worst Case Holdover Table in [µs] with asymmetrical external temperature variation (0.8°C/hour) at beginning of cycle.

dT / Holdover Time (Hour)	3°C	10°C	20°C	unit
1	0.01	0.01	0.01	µs
6	0.2	0.2	0.3	µs
12	0.6	1.0	1.0	µs
18	1.0	2.0	2.2	µs
24	1.5	3.1	4.0	µs

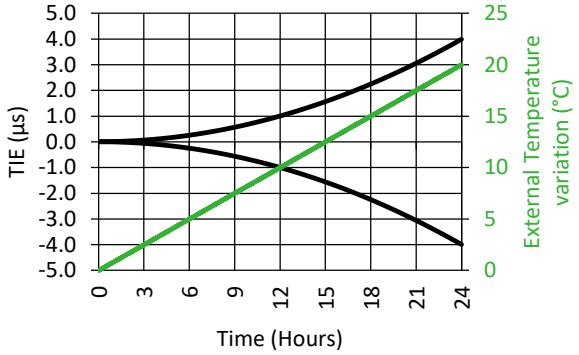
Holdover performance with ΔT = 3°C



Holdover performance with ΔT = 10°C



Holdover performance with ΔT = 20°C



16.0 I²C Bus Interface

Signal Name	Type	Function	Notes	Logic Levels
I²C Data	Tristate Input/Output	Serial Data	Min 2kΩ external Pull-Up resistor to be connected to +4V, conform to UM10204 NXP I²C-bus specification	While input to ROD3827T2 : 3.3V < V_{IH} (High) < 4.3V V_{IL} (Low) < 0.4V While output from ROD3827T2 : V_{OL} < 0.4V V_{OH} = OPEN
I²C Clock	Tristate Input	Serial Clock	Min 2kΩ external Pull-Up resistor to be connected to +4V, conform to UM10204 NXP I²C-bus specification	3.3V < V_{IH} (High) < 4.3V V_{IL} (Low) < 0.4V
Frequency			100kHz min - 400kHz max	

Note : At start up, the module performs a self-calibration process after it detects one pulse on PPS input. The self-calibration process may last 1 minute maxi. During this time the I²C is not available.

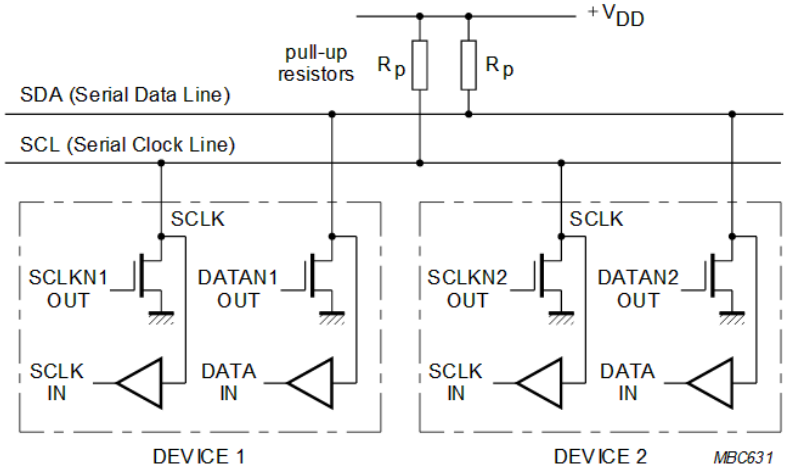
I²C Communication Conditions

I²C is not able to communicate in full-duplex mode, i.e. TX and RX are mutually exclusive. Rakon PPS Module acts as a slave in the communication setup, therefore they cannot initiate data transfers on their own. The host, which is always master, provides the data clock (SCL), and the clock frequency is therefore not configurable on the slave.

The I²C module is compliant with the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1. Fast mode up to 400 kbit/s. Fast-mode devices are downwards compatible i.e. they can be used in a 0 to 100 kbit/s Standard I²C-bus system.

Only two bus lines and a ground reference are required; a serial data line (SDA) and a serial clock line (SCL). The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.

Master must handle clock stretching feature as stated in the Philips Semiconductors Inter-IC bus (I²C-bus) specification version 2.1 as I²C data might be delayed in case of critical timing sensitive computation.

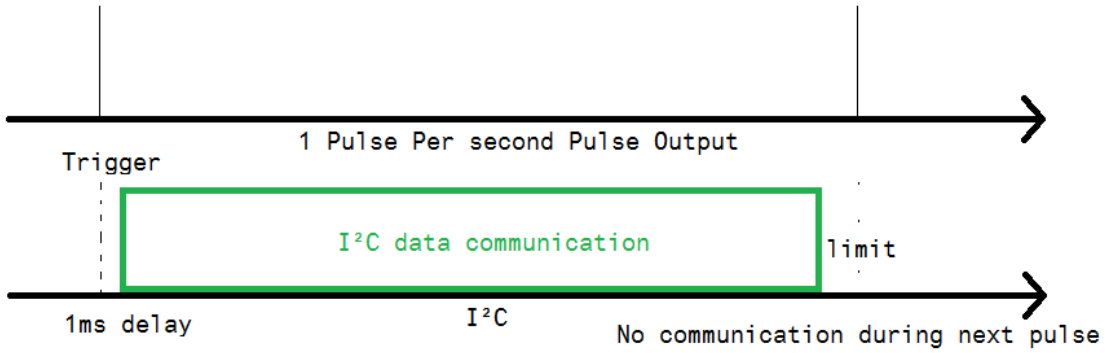


Connection of Standard- and Fast-mode devices to the I²C-bus.

Recommendation Note : 1pps output stability

In order to mitigate any synchronization issues, it is highly recommended to use the PPS output as a trigger for all I²C queries. Having an I²C communication at the same time as phase measurement is performed or generation of PPS output is done might affect product performances.

Trigger all requests that need to be done after the 1PPS output is available. This doesn't affect I²C queries on other product which are dealt on the same bus.



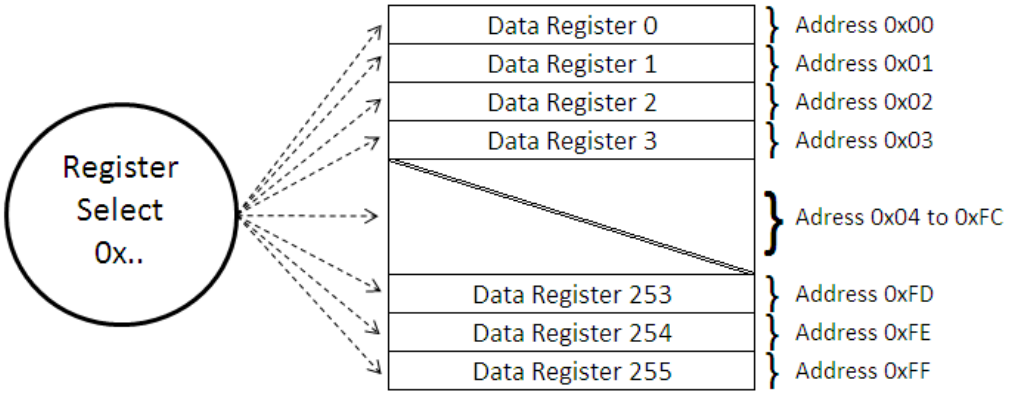
It is generally known that the I²C bus can hang if an I²C master is removed from the bus in the middle of a data read. This can occur because the I2C protocol does not mandate a minimum clock rate. Therefore, if a master is reset in the middle of a read while a slave is driving the data line low, the slave will continue driving the data line low while it waits for the next clock edge.

This prevents bus masters from initiating transfers. If this condition is detected, the following three steps will clear the bus hang condition:

1. An I²C master must generate up to 9 clock cycles.
2. After each clock cycle, the data pin must be observed to determine whether it has gone high while the clock is high.
3. As soon as the data pin is observed high, the master can initiate a start condition.

The receiver's I²C address is set to **0xE0** by default. This address can be changed on request.

The I²C interface allows 256 slave registers to be addressed. As shown in Figure *I²C Register Layout* only a few of these are currently implemented. Others are reserved for future uses or internal computation and must not be addressed.



I2C Register Layout

Register detail

Next information will procure details regarding Rakon module register.

Slave Register: Refers to the address that has to be sent after the I²C slave address to select the desired register.

Description: Name and function of the register.

Firmware: Details on the firmware revision the register is supported on.

Comment: Additional information regarding the register or the data it represents.

Message Info: Number of bytes to be read and data type of the data register.

Slave Register	**0x3E**		
Description	Read Temperature Sensor		
Firmware	1.4+		
Comment	Represents an image of the external temperature seen by the module. The value can vary from Ox0000 to Ox0FFF, negative slope		
Message Info	# bytes	Datatype	
	2	U-Short	

Slave Register	**0x41**		
Description	Read Frequency Control		
Firmware	1.4+		
Comment	Range can swing from Ox00000000 to Ox000F4240. 8E-13 typical frequency variation per step		
Message Info	# bytes	Datatype	
	4	U-Long	

Slave Register	**0x42**		
Description	Read Status		
Firmware	1.4+		
Comment	Gives information regarding the mode of the module and other parameters. Refer to Figure Status Details for more informations.		
Message Info	# bytes	Datatype	
	2	Char	

Slave Register	**0x50**		
Description	Read Product Identification		
Firmware	1.4+		
Comment	Product traceability information ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x51**		
Description	Read firmware revision		
Firmware	1.4+		
Comment	Includes the name, version revision, release date and special parameters. ASCII format		
Message Info	# bytes	Datatype	
	64	Char	

Slave Register	**0x52**		
Description	Read Relative Time Interval Error		
Firmware	1.4+		
Comment	Time Interval Error in nanosecond with an offset of +2000ns. Only available when system is locked and phase measurement is available. When there is no PPS measurement, system phase equivalent ageing is displayed. Ox0000 to Ox0FFF		
Message Info	# bytes	Datatype	
	2	U-Short	

Status detail

status channel is a bitfield information as shown below :

Byte MSB								Byte LSB						
0	0	0	0	0	0	0	0	0	/P.Out	Syst.F	1	HV	Lock Status	IsPPS

MSB byte is always 0x00

0	Must be 0 for normal operation.
/P.Out	0 : PPS ready and available on PPS_Out Pin D. 1: PPS not ready and not available on PPS_Out Pin D.
Syst.F	System Fail check. If PPS has been provided.
1	Must be 1 for normal operation.
HV	1 : Holdover Mode, no PPS detected. 0 : not in Holdover mode, PPS detected
Lock Status	b00 : System just started (power on mode, free run mode) b01 : 30s to 30mn since system started – Stabilization (run1 mode) b10 : System ready for use (Run2 mode)
IsPPS	Is there a valid PPS input ? 0: No / 1: Yes

Write Access:

The receiver does not provide any write access.

17.0 Pin Connections

Parameter	Description
Pin 1	SCL
Pin 2	SDA
Pin 3	Supply Voltage (Vcc)
Pin 4	RF Signal Output
Pin 5	GND (mechanical and supply)
Pin D	PPS out
Pin E	PPS in

18.0 Marking

Parameter	Description
Type	Label marked
Barcode	Data matrix
Line 1	RAKON (or Customer's Logo / Name)
Line 2	STP **tbd** LF
Line 3	10 MHz
Line 4	[SN: Lnnnnn] = serial number (letter + 5 numerals)
Line 5	[DC: yyww] = 4 Digits for date-code year / week

19.0 Manufacturing Information

Parameter	Description
Soldering	Hand or wave soldering
Assembly condition	Do not solder during upside down placement without mechanical fixation
Packaging description	All quantities will be provided in boxes
Moisture Sensitivity Level	MSL1 – Hermetically sealed package
Shelf life	No detrimental effect from a long shelf life (over 1 year). However, device requires 2 weeks max. of continuous operation prior to recovering its stability versus time (ageing).

20.0 Environmental Specification[2]

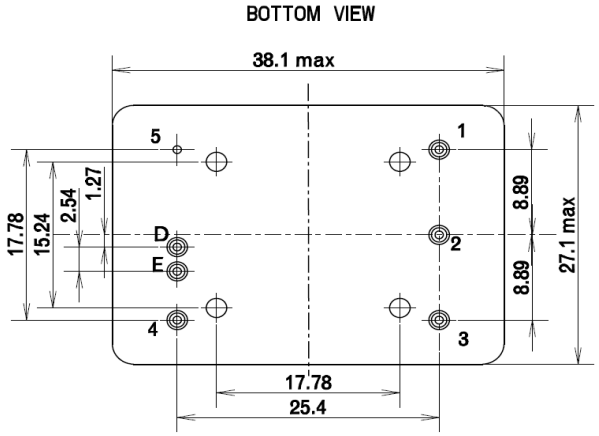
Parameter	Description
RoHS	Parts are fully compliant with the European Union directives 2002/95/EC and 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and equipment, with exemption 7(c)-1
Shock	IEC 68-2-27 Test Ea (50g, 11ms, ½ sine. 5 directions x 3 shocks)
Vibration	IEC 68-2-06 Test Fc (10g, 10-500Hz 30 minutes/axis 1.5 hour total)

[2] For qualification, not operational

21.0 Disclaimer

Parameter	Description
Disclaimer	"Samples supplied according to this specification are supplied from our development or pre-production programme and as such are not qualification approved products. No condition, warranty or representation regarding quality, suitability, performance, life or continuation of supply is given or implied and Guarantee in clause 6.1 of our standard Conditions of Sale is not applicable. The right is reserved to change the design or specification or cease supply without notice." – RAKON Limited.

22.0 Model Outline: ROD3827T2



1- I²C Clock
2- I²C Data
3- Power Supply Input (+5.0V)
4- RF Ouput Signal (10MHz)
5- Ground (mechanical and supply)
D- PPS output
E- PPS input

Note : dimples are made of glass

Pins length L= 3.30 ± 0.25 mm

23.0 Applications Notes

- Application Note :
  - 093186 - RAKON EVK Hardware Installation Guide
  - 093187- RAKON EVK Software User Guide
- Evaluation Kit ref : 516256 (ROD3827T2 EVK)

24.0 Specification History

Version	User	Changes	Approver	Date
-	Vincent CANDELIER Didier THORAX	Generic specification / draft to be validated zith customer	Claude TRIALOUP Frédéric VITTRANT	2020-02-27